Amendments to the Claims:

The listing of claims will replace all prior version, and listings, of claims in the application.

Claims 1-11 were previously cancelled without prejudice.

Claims 12-31 are cancelled herein without prejudice.

Claims 32-52 are submitted presently by way of this Amendment.

Listing of Claims:

1-11. (canceled)

Please cancel claims 12-31.

Please add new claims 32-52 as follows:

32. (newly presented) A method of comparing a data key to a rule, wherein the data key and rule are representable by bits, the method including:

generating a mask that indicates relevant bits that are relevant to identify the rule and do not care bits that are extraneous for identifying the rule;

generating a vector comprised of memory positions and at least a corresponding bit for each of the memory positions, by setting bits for those memory positions of the vector pointed to by bits of the rule when read as an address, the address including both relevant bits and do not care bits, to a value that indicates that the rule is detected;

inserting values of the bits of the vector into memory positions of a memory corresponding to the memory positions for each bit of the vector;

dividing the bits of the data key into a plurality of chunks;

extracting data from the memory at an address corresponding to the value of each of at least some of the chunks; and

examining the data extracted from each memory address corresponding to the at least some of the chunks to determine if the rule is obeyed for the entire data key.

33. (newly presented) The method of claim 32, wherein the step of generating a vector comprises automatically setting the value of the corresponding bits of the vector to indicate that the rule is detected according to the following function:

Rule[I][C bits] AND Mask[I][C bits] is equal to Mask[C bits] AND J,

wherein I is the Ith rule, C is the number of bits in a chunk, and J ranges from 0 to 2^C -1.

34. (newly presented) The method of claim 33, wherein the step of generating a mask generates a string of bits corresponding to the number of bits in a rule, and sets each bit in the mask that corresponds to a bit in the rule that is relevant for identifying that rule.

35. (newly presented) The method according to claim 32, wherein the step of generating a vector comprises setting the value of bits corresponding to a number of bits comprising a chunk.

36. (newly presented) The method according to claim 32, further comprising the step of configuring the memory into a two dimensional memory structure, a first dimension corresponding to the chunks of the data key and a second dimension corresponding to different rules.

37. (newly presented) The method according to claim 32, wherein examining the data further comprises performing at least one AND operation on the data extracted from the memory corresponding to each of the chunks of the data key to determine if the rule is obeyed for the entire data key.

38. (newly presented) The method according to claim 32, further comprising the step of providing the memory as separate memory devices and allocating sub sets of the different memory devices based on the number of rules to be detected.

39. (newly presented) The method according to claim 32, wherein a number of rules are detected, further comprising the step of prioritizing the rules according to a predetermined order of priority for rules.

40. (newly presented) The method according to claim 32, further comprising the step of parsing for parsing a packet received over a network into a data key.

41. (newly presented) The method according to claim 40, further comprising the step of receiving the packet from an Internet based network.

42. (newly presented) A system for comparing a data key to a rule, wherein the data key and rule are representable by bits, the system including:

a memory comprised of memory positions and at least a corresponding bit for each of the memory positions making up a vector, wherein bits for those memory positions of the vector pointed to by bits of the rule when read as an address, the address including both relevant bits and do not care bits, are set to a value that indicates that the rule is detected;

an interface that divides the bits of the data key into a plurality of chunks;

a comparator that compares data from each memory address corresponding to the at least some of the chunks to determine if the rule is obeyed for the entire data key.

43. (newly presented) The system of claim 42, wherein the memory is populated with the

by setting the value of the corresponding bits of the vector stored in memory to indicate that the rule is detected according to the following function:

Rule[I][C bits] AND Mask[I][C bits] is equal to Mask[C bits] AND J,

wherein I is the Ith rule, C is the number of bits in a chunk, and J ranges from 0 to 2^C -1, and wherein Mask are bits set to a value indicating relevant bits that are relevant to identify the rule and do not care bits that are extraneous for identifying the rule.

44. (newly presented) The system of claim 43, further comprising a mask formed of a string of bits corresponding to the number of bits in a rule, and sets each bit in the mask that corresponds to a bit in the rule that is relevant for identifying that rule.

45. (newly presented) The system according to claim 42, wherein the memory stores the value of bits of the vector corresponding to a number of bits comprising a chunk.

46. (newly presented) The system according to claim 42, wherein the memory is configured into a two dimensional memory structure, a first dimension corresponding to the chunks of the data key and a second dimension corresponding to different rules.

47. (newly presented) The system according to claim 42, wherein the comparator includes at least one AND device that operates on data extracted from the memory corresponding to each of the chunks of the data key to determine if the rule is obeyed for the entire data key.

48. (newly presented) The system according to claim 42, wherein the memory is provided as separate memory devices and further comprising a switch that allocates the which memory devices are grouped together based on the number of rules to be detected.

49. (newly presented) The system according to claim 42, wherein a number of rules are detected, further comprising a prioritzer that prioritizes rules according to a predetermined order of priority for rules.

50. (newly presented) The system according to claim 42, further comprising a parser for parsing a packet received over a network into a data key.

51. (newly presented) The system according to claim 50, wherein the parser receives the packet from an Internet based network.

52. (newly presented) The system of claim 42, wherein the memory includes only a number of individual memory units (per bit) according to the formula:

$$NM/(2^C L^2 C),$$

Wherein, N is the number of bits in the data key, M is the number of rules available for detection, C is the number of bits in a chunk and L is the width of a discrete memory device.